|  |  |
| --- | --- |
| Name: Abdullah Nadeem Waraich | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-126 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

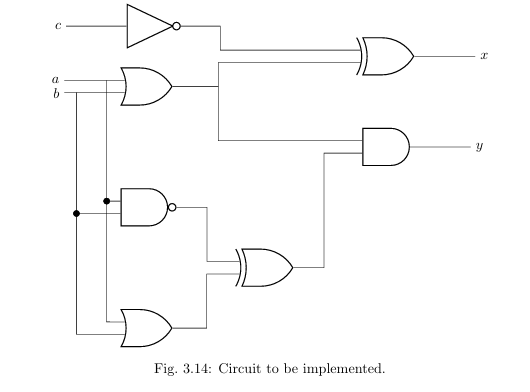
**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

# Lab Assignment 2

## Combinational Circuits: Structural Modeling using Vivado

**Circuit to be implemented :**



**PART 1:**

**Results and Findings:**

1. Truth table of circuit:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Local Signals** | | | | **Outputs** | |
| **a** | **b** | **c** | **Or\_out** | **Not\_out** | **Nand\_out** | **Xor\_out** | **x** | **y** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

1. Errors Found and Fixed:

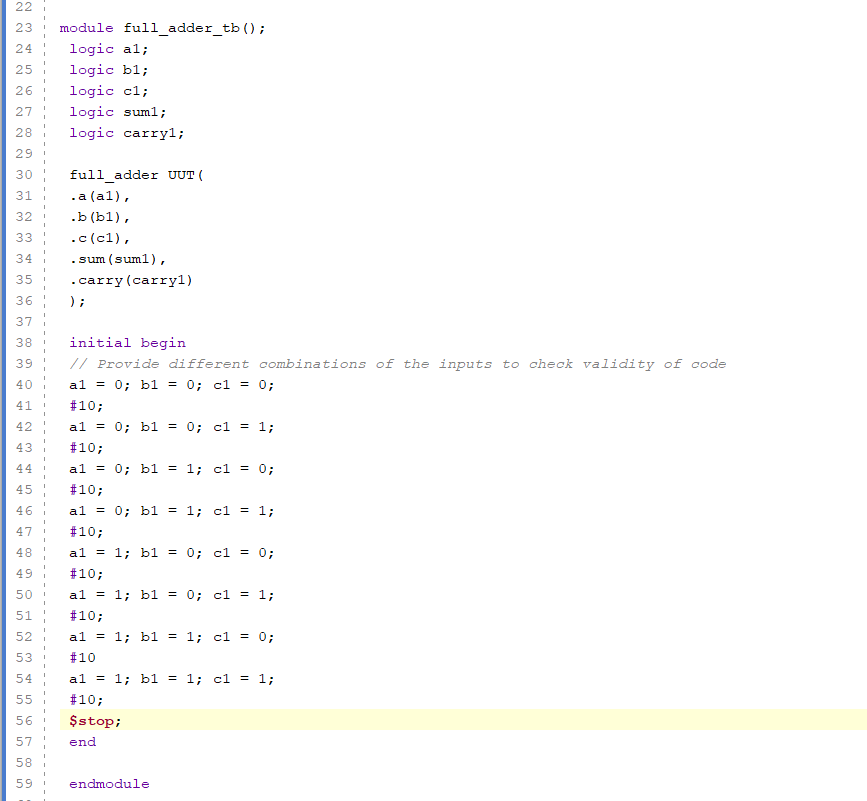
For Full adder Code:

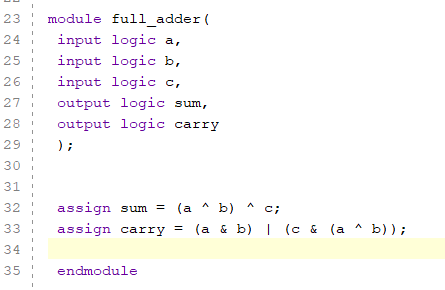
* Added Assign value before sum
* Added & between c and (a ^ b)

For Full adder Test Bench:

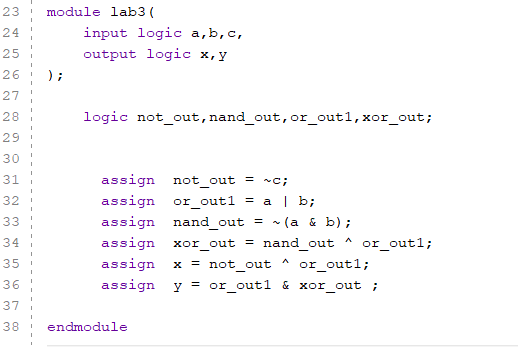
* Added local variable carry1
* Added UUT after full\_adder
* Fixed variables which were assigned only a,b,c to a1,b1,c1
* Added end to the initial begin

(c)

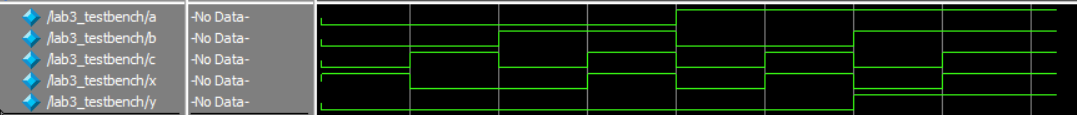




**Part 2:**

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**Part 3:**

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